

GigE Vision® IP core XILINX

GigE® compliant IP core for Spartan, Virtex, Kintex and ZYNQ devices

GigE Vision® is a standardized communication protocol for vision applications based on the well known Ethernet technology. It allows easy interfacing between GigE Vision® devices and PCs running TCP/IP protocol.

Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products with Gigabit Ethernet interface.

In principle there are two possibilities to realize systems with Gigabit Ethernet interfaces:

- use processor with
 Gigabit Ethernet interface
- use hardware based solution

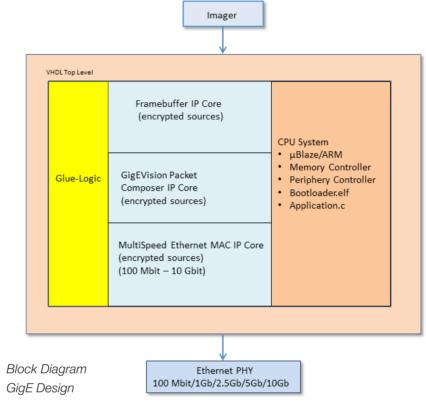
Sensor to Image developed a mixture of both concepts to combine advantages and avoid disadvantages of each approach.

This solution consists of a set of FPGA IP cores, which allow a maximum in performance at a small footprint and enough flexibility to realize custom solutions.

The following components are part of the design:

Top Level Design, which builds the interface between real hardware (e.g. sensor, external CPU, Ethernet Physical) and internal data processing. This module is delivered in source-code (VHDL), so it can be adapted and extended to custom hardware.

Memory Controller for different memory types, which allows frame buffering and image partitioning. This



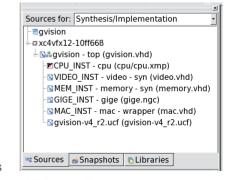
is necessary to realize the packet resend function.

The GigE Packet Composer sends all data to the Ethernet MAC and realizes the high speed "Streaming Channel" GVSP according to the GigE Vision® specification.

An FPGA integrated CPU (ARM or MicroBlaze) is for several non time critical network and configuration tasks and it runs the "Control Channel" GVCP. Software is written in C and can be extended by the customer. Some software parts are delivered as compiled files only (e.g. bootloader, GigE-controller), other parts are in source code.

The delivered design framework comes with all necessary design files and cores, ISE or VIVADO project files and a Gigabit Ethernet camera system with Xilinx FPGA and CMOS imager. This system should be used as reference design and evaluation board.

As development environment the Xilinx ISE or VIVADO is used (not in scope of delivery).



ISE Project Tree



AVAILABLE MODULES			
MODULE	COMMENT	SPARTAN 3/6	A7, K7*, ZYNQ
Sync. bus as sensor interface	incl. 1 single tap sensor adaption incl. I ² C/SPI core + C code	•	•
GigE Core	project licence for CPU interface, packet composer, MAC interface, packet resend including DDRx controller on AXI interface	•	•
Tri Mode MAC	Ethernet MAC core, only full-duplex supported	•	•
GigE Vision/GenlCam software	SPHINX image viewer incl. filter driver, Transport Layer API, XML-File generation (seperate product of Sensor to Image GmbH)	•	•
Full sources, design,	on request		
* A7: Artix-7, K7: Kintex-7		other FF	GA vendors on request

RESOURCES					
MODULE (S3/6 ISE PLB, 7 SERIES VIVADO-AXI)	SPARTAN-6	VIRTEX-6	ARTIX-7	KINTEX-7	ZYNQ
GigE Packet Composer					
- Slice registers	3542	3549	3441	3201	3229
- Slice lookup tables	4058	4151	3800	3587	3651
- Block RAMs	11	6	9	4	4
- Maximum clock frequency**	155 MHz	221 MHz	172 MHz	225 MHz	201 MHz
Framebuffer					
- Slice registers	2486	2416	5973	2076	2198
- Slice lookup tables	2266	2197	5107	1835	1877
- Block RAMs	1	1	2	2	2
– Maximum clock frequency	188 MHz	276 MHz	229 MHz	282 MHz	233 MHz
CPU system based on MicroBlaze processor					
- Slice registers	2797	4750	18458	4189	4240
- Slice lookup tables	2959	4264	21494	3766	3864
- BlockRAMs	14	16	10	8	8
- Minimum clock frequency	62.5 MHz	62.5 MHz	62.5 MHz	62.5 MHz	62.5 MHz
MAC					
- eMACs	-	1	-	-	-
- Slice registers	599	_	710	513	584
- Slice lookup tables	676	_	792	587	652
- BlockRAMs	-	-	0	-	-
- Maximum clock frequency	125 MHz	125 MHz	125 MHz	125 MHz	125 MHz
** 62.5 MHz required to reach maximum bandwidth of Gigabit Ethernet					

values are post synthesize only and based on platform specific reference designs, other architectures might have different resource usage

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